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Karen Vertz		(Depositor's name)
Karen Vertz		(Signature)
4-22-040		(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,514	07/29/2003	Craig T. Salling	TI-32206.1'	6919

TITLE OF INVENTION: METHOD TO INCREASE SUBSTRATE POTENTIAL IN MOS TRANSISTORS USED IN ESD PROTECTION CIRCUITS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	07/16/2004
EXAMINER		ART UNIT		CLASS-SUBCLASS	
HOGANS, DAVID L		2813		438-527000	

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1. W. James Brady, III

2 Frederick J. Telecky, Jr.

3.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant Craig T. Salling, et al.

Docket Number: TI-32206.1

Serial No.: 10/629,514

Art Unit: 2813

Filed: 07/29/03

Examiner: David L. Hogans

For: Method to Increase Substrate Potential in MOS Transistors
Used in ESD Protection Circuits

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NAME OF INVENTOR(S):	
Craig T. Salling, et al.	
TITLE OF INVENTION: Method to Increase Substrate Potential in MOS Transistors Used in ESD Protection Circuits	
TI FILE NO.:	DEPOSIT ACCT. NO.:
TI-32206.1	20-0668
FAXED: 4-22-04 DUE: 7-18-04 ATTY/SECY: GCH/kjv	
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